Amendments to the Drawings:

Please enter the attached drawing Replacement Sheet, which is being provided with a complete set of the drawings. The replacement sheet includes a revised FIG. 11, which is revised to replace "XOR 218" with "XOR 332".

REMARKS

Claims 1-11, 13-20, and 22-28 are in the application of which claims 1, 10, 16, and 23 are in independent form.

The Examiner is thanked for his careful attention to the specification and drawings. Various amendments (described below) are made to the specification and drawings to correct minor mistakes. No new matter is added.

Drawings. The drawings are objected to because the number "218" in FIG. 11 should be "332." The correction is made in a replacement sheet included with the complete set of drawings.

Abstract.

The abstract (paragraph at page 25) is amended to remove the sentence "Still other embodiments are described and claimed." However, it should be clear that the disclosure and inventions are not restricted by the details of the abstract.

Disclosure.

The paragraph at page 2, lines 4-7, is amended to include reference to application no. 10/625,945 and its filing date.

The specification is amended in the paragraphs at page 16, lines 12-16; page 16, lines 17-25; page 16, line 26 - page 17, line 3; page 17, lines 16-20, and page 17, lines 21-25 to correct mistakes in the description.

The Office action mentions that correction is needed for the paragraph at page 17, lines 11-15. The undersigned attorney was unable to identify a problem with this paragraph. The Examiner is requested to call the undersigned attorney and seek an examiners amendment for any defect in it.

Claim objections. Claims 10-15 and 23-28 are objected to because of informalities.

Claim 10, line 4 is amended as suggested.

Claims 10, 12, 13, 15, 23, and 24 are objected to for using the phrase "cycle encoded signal" rather than "full cycle encoded signal." The specification, page 5, lines 11-19, states:

"The inventions described herein include a system having a transmitter that encodes a data signal into a cycle encoded signal (CES). * * * In a CES, at least some of the data time segments do not include more than one cycle of a particular encoding signal. In a full CES, no data time segment has more than one cycle of an encoding signal. In a partial CES, some data time segments have more than one cycle of an encoding signal, and other data time segments do not have more than one cycle of an encoding signal."

Consistent with the specification, claims 10, 12, 13, 15, 23, and 24 recite "cycle encoded signals" without specifying whether they are full cycle encoded signals or partial cycle encoded signals. Dependent claims 11 and 28 further limit claims 10 and 23 by stating "wherein the cycle encoded signal is a full cycle encoded signal ...."

Since the specification indicates there may be "cycle encoded signals" that are not "full cycle encoded signals," it is believed that claims 10 and 23 do not have to be restricted to including "full cycle encoded signals."

Claim 27, line 1, and also claim 16, line 1, are amended to changed "receiver that includes" to "receiver includes".

Claims 11 and 28 are not canceled since they further limit claims 10 and 23.

Since independent claims 10 and 23 are addressed above, it is believed that dependent claims 14, 25, 26, and 28 need not be further addressed.

35 U.S.C. 112, first paragraph. Claims 9, 15, and 22 are rejected under 35 U.S.C. 112, first paragraph, as being non-enabling.

Claims 9 and 15 are amended to recite: "a data out signal which ~~recovers~~ includes recovered data from ~~another~~ the cycle encoded signal."

Claim 22 recites: "wherein the recovered values are the inverse of those of the data input signal." This is supported by the specification at page 5, lines 25-26, which states: "The inventions also include receivers to receive the CES, and in some embodiments the CCES, and recover the data or, in some embodiments, an inverse of it." (Emphasis added.). For example, in FIG. 4, there is a "data out" signal and a "data out*" signal, where data out* is the inverse of data out. The inverse can be obtained by merely using data out* rather than data out. This is explained in the specification at page 12, lines 26-29:

"As can be seen, the value of the data out signal follows the value of the CES and CCES signals with a delay as described. As mentioned, with different logic the data out signal could have the opposite value. Further, the receiver could use the data out* signal (which is the inverse of the data out signal) in place of the data out signal, if desired."

35 U.S.C. 112, second paragraph. Claims 9, 15, 21-22, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claims 9, 15, and 27 are amended to recite inter-relationships between the initial receiving

circuit, delay circuit and logic circuit, such as is shown, for example, in FIG. 3. Claim 21 is canceled and incorporated into claim 16 with the additions that are in claims 9, 15, and 27. Claim 22 now depends on claim 16.

Double Patenting. Claims 23, 26, and 30 are provisionally rejected for non-statutory double patenting over claims 28-30 of copending Application No. 10/625,944.

Without conceding the correctness of this rejection, a terminal disclaimer is provided herewith.

35 U.S.C. 102(b). Claims 1, 4-8, 10-11, 14, 16, 19, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Pfiffner (U.S. Patent No. 5,623,518).

The Office action, page 9, indicates that claims 2-3, 12-13, 17-18, 21 and 23-28 include some allowable subject matter assuming 35 U.S.C. 112 and double patenting issues are resolved.

Claim 1 is amended to include objected to claim 3 except for the last phrase of claim 3, which remains in claims 3. As amended, claim 1 recites:

"wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal."

Nothing in Pfiffner shows such a multiplexer that selects which encoding signal to pass. Rather, in Pfiffner, a CPU (FIG. 2A) or a DSP (FIGS. 2B - 2D) provides the signal, but does not select from different existing encoding signals. Accordingly, claim 1 should be allowed.

Claims 2-9 are dependent on claim 1 and should be allowed for at least that reason.

Claim 10 is amend to include limitations of objected to claim 12, which is no canceled. Claims 11 and 13-15 are dependent on claim 10 and should be allowed for at least that reason.

Claim 16 is amend to include limitations of objected to claim 21 which are expanded to provide additional details to connect the initial receiver circuit, delay circuit, and logic circuit. Claim 21 is canceled Claims 17-20 and 22 are dependent on claim 16 and should be allowed for at least that reason.

Allowance of the application is respectfully requested.

Respectfully submitted,

Dated: January 17, 2007

Alan K. Aldous
Reg. No. 31,905
Attorney for Intel Corporation

Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026
Phone: (503) 372-1066
Phone: (503) 439-8778
Phone (310) 207-3800
Facsimile: (503) 439-6073